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(54) **Data transmitting-receiving system.**

(57) A data transmitting-receiving system includes a transmitter unit (100), a receiver unit (200), and a transmission line (137) connected therebetween. The transmitter unit includes conversion means (111-113; 121-123) to convert digital input data (D1, D2) of each of two channel routes into analog output signals (A1, A2), a respective modulator (115, 125) in each channel route driven by the respective analog output signal, and means (133-136) to add the outputs from the modulators and to transmit the resultant signal to the receiver unit via the transmission line. Each conversion means includes a memory circuit (111, 121) which receives the digital input data, and a digital/analog (D/A) converter (113, 123) which converts a digital output (d11, d21) from the memory circuit into the analog output signal. Each memory circuit provides a digital output (d11, d21) corresponding to the respective digital input data and also provides predetermined digital correction outputs (d12, d22) dependent upon the values of the individual input data. Each digital correction output comprises digital correction outputs related respectively to the own-side channel route and the other-side channel route. Each D/A converter produces the respective analog output signal taking into account the digital correction output related to the respective own-side channel route and the digital correction output from the other-side channel route. By use of the digital correction signals, non-linearity and modulation distortion in the system are cancelled out.

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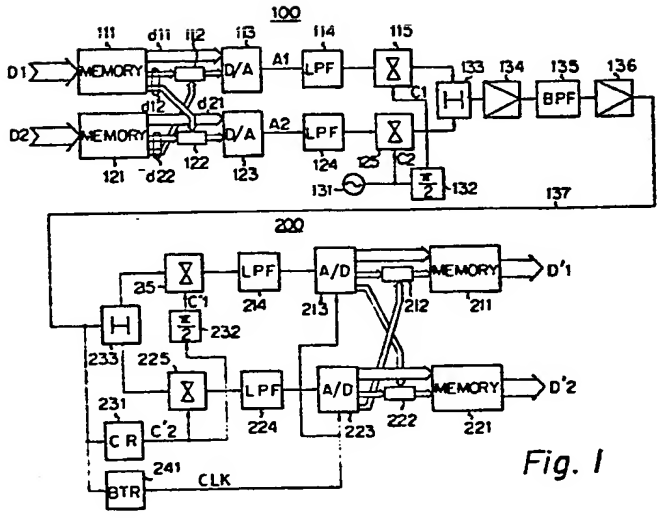

100
111
d11
112
113
114
115
D1
MEMORY
D/A
A1
LPF
C1
133
134
135
136
BPF
d12
d21
D2
MEMORY
D/A
A2
LPF
C2
121
d22
122
123
124
125
131
π/2
132
137
200
25
C'1
LPF
214
A/D
213
MEMORY
211
D'1
212
H
π/2
232
233
225
231
C'2
LPF
224
A/D
223
222
MEMORY
221
D'2
C R
241
CLK
BTR

Fig. 1

DATA TRANSMITTING-RECEIVING SYSTEM

This invention relates to a data transmitting-receiving system.

Various systems are used for transmitting and receiving data and, whichever system is employed, attention must be paid to the reliability of the data.

A known data transmitting-receiving system comprises a transmitter unit and a receiver unit interconnected via a transmission line. The transmitter unit comprises a first level converter which produces an analog level signal according to the combination of first digital input data of a plurality of channels allotted to a first channel route; a first mixer which receives, at its first input, a first analog output from the first level converter and, at its second input, a first carrier; a second level converter which produces an analog level signal according to the combination of second digital input data of a plurality of channels allotted to a second channel route; a second mixer which receives, at its first input, a second analog output from the second level converter and, at its second input, a second carrier; a hybrid circuit which adds the analog outputs of the first and second mixers; and an amplifier for amplifying the output from the hybrid circuit to a transmission power level.

The receiver unit comprises a first demodulator and a second demodulator which reproduce transmission signals corresponding to the first and second channel routes, respectively, and then demodulate the thus-reproduced analog level signals into first digital output data and second digital output data, respectively.

In the above prior art system, various factors cause data errors. The factors are, for example, non-

-linearity of the amplifier in the transmitter unit, modulation distortion of the mixer in the transmitter unit, temperature variation, and ageing of the system itself. Many proposals have been made for coping with these problems individually to improve data reliability, but few proposals have been made for dealing with all of these problems at once.

It is an object of the present invention to provide a data transmitting-receiving system which can deal with the various factors causing data errors.

According to the present invention, there is provided a data transmitting-receiving system, including a transmitter unit, a receiver unit, and a transmission line connected therebetween, the transmitter unit including conversion means to convert digital input data of each of two channel routes into analog output signals, a modulator in each channel route driven by the respective analog output signal, and means to add the outputs from the modulators and to transmit the resultant signal to the receiver unit via the transmission line; characterised in that each conversion means includes a memory circuit to receive the digital input data, and a digital/analog (D/A) converter to convert a digital output from the memory circuit into the analog output signal; in that each memory circuit provides a digital output corresponding to the respective digital input data and also predetermined digital correction outputs dependent upon the values of the individual input data, the digital correction outputs comprising digital correction outputs related respectively to the own-side channel route and the other-side channel route; and in that each D/A converter is operative to produce the respective analog output signal taking into account the digital correction output related to the respective own-side channel route and the digital correction output from the other-side channel route.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which

Fig.1 is a block diagram of a data transmitting-receiving system according to the present invention;

Fig.2 is a graph of input-output characteristics of an amplifier for transmission forming part of the system of Fig.1;

Fig.3 is a vector diagram of the distribution of data coded in a 64-value quadrature amplitude modulation method;

Fig.4 illustrates an example of a memory circuit provided with data buses;

Fig.5 is a block diagram of an example of major portions for suppression of data-error in the system of Fig.1; and

Fig.6 illustrates another example of a data-error supervising circuit forming part of the system of Fig.5.

Referring to Fig.1, a data transmitting-receiving system comprises a transmitter unit 100, a receiver unit 200, and a transmission line 137 interconnecting the units. The transmission line 137 may be a microwave line, a millimetric wave line, or a cable line. Reference character D1 denotes digital input data of a first channel route, which are usually composed of multiplexed data of a plurality of channels. A memory 111, an adder 112 and a digital/analog converter 113 together form a first level converter from which an analog level signal is produced in accordance with various combinations of the plurality of channel digital input data, such as "1" "0" "1" and "0" "1" "1" in the case of three channels. A first analog output A1 from the first level converter (111,112,113) is applied via a low-pass filter (LPF) 114 to a first mixer 115 at its first input. The low-pass filter 114 is used for spectrum shaping of output signals.

A carrier generator 131 produces a carrier signal C1 which is fed to phase shifter ($\pi/2$) 132, and thence to

the second input of the first mixer 115 as a first carrier C1. Modulation is thereby performed by the first mixer 115 on the first analog output A1 at its first input.

On the other hand, a reference character D2 denotes digital input data of a second channel route, which are usually composed of multiplexed data of a plurality of channels, as are the data D1. The description of the operations for the data D1 also apply to the data D2. Reference numerals relating to the data D2 bear a second digit of "2" instead of "1". The carrier signal from the generator 131 is fed to a second mixer 125 as a carrier C2 without phase shift, so that the second carrier C2 is $\pi/2$ out of phase with the first carrier C1.

The analog outputs from the first mixer 115 and the second mixer 125 are added to each other at a hybrid circuit (H) 133. The added output is then transferred, via an intermediate frequency (IF) amplifier 134 and a band-pass filter (BPF) 135, to a high-power amplifier 136 and is amplified therein to a transmission power level. The thus-amplified transmission signal is fed,via the transmission line 137,to the receiver unit 200. The transmission signal is branched at a hybrid circuit 233. The branched signals are reproduced by a first receiving-end mixer 215 and a second receiving-end mixer 225 into a first channel route signal and a second channel route signal, respectively. In this reproducing operation, a first recovery carrier C'1 and a second recovery carrier C'2 are used. The carrier C'2 is produced at a carrier recovery circuit (CR) 231 and the carrier C'1 is produced therefrom by way of a phase shifter ($\pi/2$) 232. The outputs from the mixers 215 and 225 are applied, via low-pass filters 214 and 224, to a first demodulator comprising an A/D converter 213, an adder 212 and a memory 211, and a second demodulator comprising an A/D converter 223, an adder 222 and a memory 221, so that the original data are demodulated to obtain first digital

output data D'1 and second digital output data D'2, respectively.

The characterising features of the present invention in the system of Fig.1 are the first level converter (111, 112, 113), the second level converter (121,122,123), the first demodulator (213, 212, 211), and the second demodulator (223, 222, 221). It should be noted that, according to the present invention, the first and second level converters in the transmitter unit 100 should be constructed as shown in Fig.1, but it is not essential to construct the first and second demodulators in the receiver unit 200 as shown therein. The first and second demodulators may be constructed in a conventional manner.

The reason why at least the first and second level converters (111, 112, 113 and 121, 122, 123) should be constructed as shown in Fig.1 will be given below.

It should be remembered here that the object of the present invention lies in ensuring data reliability and that one of the factors causing deterioration of data reliability resides in non-linearity of the amplifier 136 in Fig.1. Figure 2 is a graph of input-output characteristics of the amplifier 136 shown in Fig.1. In the graph, the abscissa indicates a level P_{in} of the input signal, while the ordinate indicates a level P_{out} of the output signal. The relationship between the levels P_{in} and P_{out} is ideally linear. That is, the level P_{out} should vary with the level P_{in} along a line 21. In actuality, however, the level P_{out} varies with the level P_{in} along a curve 22, so that it exhibits non-linearity. This is mainly caused by a saturation phenomenon inherent to the amplifier 136.

Up to now, such non-linearity has not caused much data error and therefore could be disregarded. Referring to the data transmitting-receiving system of Fig. 1, even with some non-linearity, there is almost no likelihood of data error in the case of the usual four-value quadrature amplitude modulation, in which four digital input values ("0" "0"), ("0" "1"), ("1" "0"), and ("1" "1") are allotted to the phases of 0, $\pi/2$, π, and $3/2\pi$, respectively. Even with only a small amount of non-linearity, however, there is a likelihood of data error due to error in reading data in the case of a higher multiple value quadrature amplitude modulation method, such as 16-value, 32-value, or 64-value, adopted to cope with increased amounts of transmission data. Under such circumstances, the threshold levels for discriminating individual data necessarily become closer to each other, increasing the likelihood of reading error.

In the present invention, the actual non-linear relationship between the levels P_{in} and P_{out} is transformed by the first and second level converters of Fig.1 with a linear relationship as indicated by line 21 of Fig. 20. The first level

converter comprises a first memory circuit 111 and a first D/A converter 113. The second level converter comprises a second memory circuit 121 and a second D/A converter 123. The blocks (112, 122) located between the memory circuits and the D/A converters represent adders.

The first memory circuit 111 receives, as an address input, the first digital input data D1 and produces a first digital output d11 corresponding thereto to be applied to the first D/A converter 113. Simultaneously, the memory circuit 111 produces a first digital correction output d12 which is predetermined in relation to the first digital output d11. The output d12 is then applied, via the first adder 112, to the D/A converter 113. In this case, the first digital correction output d12 is composed of an own-side output and an other-side output. The own-side output works only for the channel route which the first digital output relates to and, therefore, is inputted to the first adder 112. The other-side output works only for the other channel route and, therefore, is inputted to the second adder 122. For the purpose of explanation, the other-side output of the digital correction output d12 will be disregarded here. A concrete explanation will be provided later. The same also applies to the other-side data of the second digital correction output d22 from the second memory circuit 121, which other-side data are to be input to the first adder 112. Thus, the first D/A converter 113 converts the combination of the first digital output d11 and the second digital correction output d22 into corresponding first analog output A1. Similarly, the second D/A converter 123 converts the combination of the second digital output d21 and the second digital correction output d22 into a corresponding second analog output A2.

The first digital output d11 is a main output whose non-linearity is not compensated. Accordingly, after

being amplified by the amplifier 136, the first digital output d11 exhibits the input-output characteristics represented, in Fig. 2, by the curve 22. To be specific, in Fig. 2, if the output d11 is fed with an input level P1 to the amplifier 136, then a non-linear (undesired) output level P3 is produced therefrom. In this case, the desired output level, i.e. the linear output level, is not the level P3, but P2. In order to obtain the linear level P2 as intended, assuming the level P_1 is inputted, it is best to use a corrected input level P4 instead of P1. The desired linear output level P2 can therefore be produced via the non-linear curve 22. It is important to note that such conversion in level from P1 to P4 is achieved with the aid of the own-side output of the first digital correction output d12. The conversion is also achieved in the second channel route with the aid of the own-side output of the second digital correction output d22. As a result, the data error, due to the non-linearity of the amplifier 136, can be eliminated by means of the memory circuits (111, 121) with respective D/A converters (113, 123).

The other-side outputs of the first and second digital correction outputs will now be explained. The other-side outputs of the first and second digital correction outputs d12 and d22 are inputted to the second and first adders 122 and 112, respectively. These other-side outputs are made available for preventing data error caused by the previously mentioned modulation distortion of the mixer.

In the data transmitting-receiving system of Fig. 1, even with some modulation distortion there is almost no likelihood of data error in the case of a usual four-value quadrature amplitude modulation in which four digital input values ("0" "0"), ("0" "1"), ("1" "0"), and ("1" "1") are allotted to the phases of 0, $\pi/2$, π, and $3/2\pi$, respectively. Even with only a little modulation distortion, however, there is a

likelihood of data error due to error in reading data in the case of a higher multivalue quadrature amplitude modulation method, such as 16-value, 32-value, or 64-value, adopted to cope with an increased amount of transmission data. Under such circumstances, the threshold levels for discriminating individual data necessarily become closer to each other, increasing the likelihood of read error. Modulation distortion of the mixer is caused by inherent characteristics of diodes which comprise the first and second mixers 115 and 125 of Fig. 1.

Figure 3 is a vector diagram of the distribution of data coded under a 64-value quadrature amplitude modulation method. In the diagram, the ordinate represents an in-phase channel (I-CH), and the abscissa a quadrature channel (Q-CH). The I-CH corresponds to, for example, the route for data D1, i.e., the first channel route, and Q-CH to the route for the data D2, i.e., the second channel route. If there were no modulation distortion in the first and second mixers 115 and 125, the 64-value coded data on the transmission line 137 would be distributed on the cross points defined by the solid line matrix and, therefore, discrimination of these data would be very easy. In actuality, however, such modulation distortion is inevitable in a mixer. Therefore, the 64-value coded data are distributed on cross points defined by the broken line matrix. As apparent from Fig. 3, since the broken line matrix is formed in a zig-zag pattern, correct discrimination of data cannot be expected. This necessarily causes data errors.

Modulation distortion can be suppressed by the present invention in the following manner. For example, in Fig. 3, suppose that certain data should be located at a coded point R1. In actuality, however, the data are unintentionally shifted to a neighbouring coded point R2 due to modulation distortion. In this case, if predetermined correction values are given to the data

represented by the thus-shifted point R2 in advance, the data can correctly be represented by the intended point R1 after cancellation of the undesired modulation distortion. It should be noted that the correction values must be given not only to own-side channel data, but also to other-side channel data. Specifically, regarding the data D1 of the first channel route (I-CH), the correction value to be given thereto in advance is not only ΔI, but also ΔQ, although the value ΔQ is not inherent to the data D1 in question, but to the data D2 of the second channel route (Q-CH).

Returning again to Fig. 1, the own-side output (inputted to the first adder 112) of the first digital correction output d12 is compensated by the correction value ΔI, while the other-side output (inputted to the first adder 112 too) of the second digital correction output d22 is compensated by the correction value ΔQ. The same also applies to the second digital input data D2. That is, the own-side output (inputted to the second adder 122) of the second digital correction output d22 works as a correction value given to the component in a direction of the Q-CH (i.e. second channel route). The other-side output (inputted to the first adder 112) of the second digital correction output d22 works as a correction value given to the component in a direction of the I-CH (i.e. first channel route). The above is schematically clarified with crossings of buses in Fig. 1, i.e. each own-side bus is connected to the other-side adder. Thus, with the use of the memory circuits 111 and 121 and the corresponding D/A converters 113 and 123, data error due to modulation distortion of the first and second mixers 115 and 125 can be prevented. Aside from non-linearity of the amplifier and modulation distortion of the mixer, data error may also be caused by temperature variation in the transmitter unit (or receiver unit). In this case, correction values to be given to the data D1

and D2 are further stored, in advance, in the first and second memory circuits 111 and 121 so as to cope with temperature variation. It should be understood that since temperature variation is not constant but changes continuously, read only memories (ROM's) are not preferable for the first and second memory circuits 111 and 121 as the circuits must be rewritten every moment. Random access memories (RAM's) are preferable since the stored data can be rewritten in response to continual detection data from a temperature sensor (not shown) every moment. Use of ROM's or RAM's, however, is a matter of choice. If only fixed data are involved, such as the aforesaid non-linearity and/or modulation distortion, the first and second memory circuits 111 and 121 may comprise ROM's.

So-called IC memories may also be used for the first and second memory circuits 111 and 121. The IC memories may be ROM's or RAM's in accordance with the service needed.

Figure 4 illustrates an example of a memory circuit provided with data buses. Here, "memory circuit" specifically refers to the first memory circuit 111. The same construction can also be applied to the second memory circuit 121. In Fig. 4, the character d11 denotes the previously-mentioned first digital output, composed of, for example, 3 bits. The character d12I denotes the own-side output of the first digital correction output d12, while d12Q denotes the other-side output of the first digital correction output d12. Each of these outputs is composed of, for example, 5 bits. Thus, there are 13 (3 + 5 + 5) bits composing the digital output from the first memory circuit 111. In this example, the memory circuit 111 is fabricated of two 8-bit memories. Such an 8-bit memory is widely marketed and, therefore, easily obtainable. It should be understood that while 3 output bits of the 8 output bits in the lower memory in Fig.4 are left unused, such

unused bits are not so disadvantageous considering the simplified memory construction.

In addition to the transmitter unit 100 (Fig.1),it is advantageous to prevent data errors in the receiver unit 200 (Fig.1) as well. In the present invention, the first demodulator comprises a first receiving-end analog/ digital (A/D) converter 213, a first receiving-end memory circuit 211, and a first receiving-end adder 212 connected therebetween. The operation of the first demodulator is the reverse of the previously-mentioned case of the first level converter in the transmitter unit,so that the first digital output data D'1 is produced. Similarly, the second demodulator comprises a second receiving-end A/D converter 223, a second receiving-end memory circuit 221, and a second receiving-end adder 222 connected therebetween. The operation of the second demodulator is the reverse of the previously-mentioned case of the second level converter in the transmitter unit, so that the second digital output data D'2 is produced. The first and second receiving-end A/D converters 213 and 223 are operated in synchronism with a clock CLK which is reproduced from the transmitted signal by means of a bit timing recovery circuit (BTR) 241.

In addition to data error prevention in the transmitter unit 100 and the receiver unit 200 as separate units, it is advantageous to prevent data errors in the overall system, i.e. the transmitter unit 100,the transmission line 137, and the receiver unit 200 as a whole. In this case, the particular factor causing the data errors is not important. The correction is effected in the system as a whole, whenever the resultant first digital output data D'1 and/ or the second resultant digital output data D'2 are found to be defective.

Fig.5 is a block diagram of an example of the main components for suppression of data errors anywhere in the system of Fig.1. In Fig.5,components which are the same as those of Fig.1 are represented by the same reference numerals

or characters. The block 55 shown at the upper right is a data-error supervising circuit (SUP) which supervises the first and second digital output data D'1 and D'2 to determine the frequency of occurrence of the data errors If the errors occur very frequently, the supervising circuit 55 triggers a central processing unit (CPU) 53 by way of a subtransmission line 56. The CPU 53 then controls, via a peripheral interface adapter (PIA) 54, both a first switch circuit (SW) 51 and a second switch circuit (SW) 52 to switch their statuses from an input data mode (D1, D2) to a test data mode (TD1, TD2). Each of the test data TD1 and TD2 has a predetermined particular data pattern. The transmitted test data TD1 and TD2 are received at the supervising circuit 55 in the form of received test data TD'1 and TD'2, respectively, and analyzed therein. The resultant analyzed information is returned, via the subtransmission line 56, to the CPU 53. The CPU 53 operates, according to the thus-returned information to output the amount of the correction values given, in advance, to the original first and second digital input data D1 and D2 so as to minimize the data error in the data D'1 and D'2. Thereafter, the first and second memory circuits 111 and 121 (both comprising RAM's) are rewritten with the thus-renewed correction values, thereby restarting usual data transmission in the system with minimum data error. At this time, the switch circuits 51 and 52 are already switched to pass usual respective data D1 and D2 therethrough. It should be understood that since the subtransmission line 56 does not have to be a high-speed transmission line, the subtransmission line 56 does not have to be a separately and newly-installed line, but may be an existing low-speed line or public line.

The data-error supervising circuit 55 of Fig. 5 can be realized, as one example, by a known parity error checker which receives both data D'1 and D'2 and carries out

the parity check therefor.

Figure 6 illustrates another example of the data--error supervising circuit 55 shown in Fig. 5. In Fig. 6, data buses 61-1 and 61-2 transfer the upper 3 bits of branched data D'1 (TD'1) and branched data D'2 (TD'2), respectively. These two sets of 3-bit data are stored, via a data bus 61, in a memory circuit 63. The lower 5 bits thereof are applied, respectively, to a first integrator 64-1 and a second integrator 64-2, via respective A/D converters (not shown). The outputs from the converters 64-1 and 64-2 are applied to a first comparator 65-1 and a second comparator 65-2, respectively.Each comparator receives a threshold level voltage V_{th}. When the transmission data include no error, the lower 5 bits thereof are usually all logic "0". However, if an error is included, bit or bits of logic "1" are very liable to occur. In the latter case, the output level from at least one of the integrators 64-1 and 64-2 exceeds the predetermined threshold level of V_{th}. If the level exceeds the level of V_{th} , the comparator 65-1 and/or the comparator 65-2 produce an output of logic "1", which logic "1" is provided through an OR gate 66, indicating that data error occurs. The data error indication signal is supplied, on one hand, to the CPU 53 (Fig. 5), via an OR gate 67 and the subtransmission line 56 and, on the other hand, to the memory circuit 63, at its write enable terminal WE, so as to put it in a write mode. When the CPU 53 receives the data error indication signal, the CPU 53, on one hand, operates to switch the switch circuits 51 and 52 (Fig. 5) to transmit the test data TD1 and TD2 instead of D1 and D2, and, on the other hand, triggers a parallel/serial converter (P/S) 68. Thus, both upper 3 bits data, i.e., main data of the received test data TD'1 and TD'2, once stored in the memory circuit 63, are returned, in the form of serial data, to the CPU 53, via the OR gate 67 and the line 56, for analysis thereby.

As explained above in detail, due to the presence, in the system of the present invention, of the memory circuits and the D/A (or A/D) converters cooperating therewith, the data transmitting-receiving system can suppress data errors and, therefore, enables high quality data communication to be achieved.

CLAIMS

1. A data transmitting-receiving system, including a transmitter unit (100), a receiver unit (200), and a transmission line (137) connected therebetween, the transmitter unit including conversion means (111-113; 121-123) to convert digital input data (D1,D2) of each of two channel routes into analog output signals (A1,A2), a modulator (115,125) in each channel route driven by the respective analog output signal, and means (133-136) to add the outputs from the modulators and to transmit the resultant signal to the receiver unit via the transmission line; characterised in that each conversion means includes a memory circuit (111,121) to receive the digital input data, and a digital/analog (D/A) converter (113,123) to convert a digital output from the memory circuit into the analog output signal; in that each memory circuit provides a digital output (d11,d21) corresponding to the respective digital input data and also predetermined digital correction outputs (d12,d22) dependent upon the values of the individual input data, the digital correction outputs comprising digital correction outputs related respectively to the own-side channel route and the other-side channel route; and in that each D/A converter is operative to produce the respective analog output signal taking into account the digital correction output related to the respective own-side channel route and the digital correction output from the other-side channel route.

2. A system as claimed in Claim 1, characterised in that a first said memory circuit (111) and a first said D/A converter (113) form a first level converter; in that the first memory circuit receives the digital input data (D1) of a first said channel route as an address input therefor and produces a corresponding first digital output (d11) to be

applied to the first D/A converter, and simultaneously supplies a first said digital correction output (d12) to the first D/A converter relating to the digital input data of the first channel route; in that a second said memory circuit (121) and a second said D/A converter (123) form a second level converter; in that the second memory circuit receives the digital input data (D2) of a second said channel route as an address input therefor and produces a corresponding second digital output (d21) to be applied to the second D/A converter, and simultaneously supplies a second said digital correction output (d22) to the second D/A converter relating to the digital input data of the second channel route; in that the first D/A converter receives the first digital output (d11) together with the first digital correction output (d12) and the second digital correction output (d22) so as to produce a first analog output signal (A1); and in that the second D/A converter receives the second digital output (d12) and the second digital correction output (d22) so as to produce a second said analog output signal (A2).

3. A system as claimed in Claim 2, characterised in that the first digital correction output (d12) from the first memory circuit (111) comprises a first own-side correction output to be applied to the first D/A converter (113) and a first other-side correction output to be applied to the second D/A converter (123); in that the second digital correction output (d22) from the second memory circuit (121) comprises a second own-side correction output to be applied to the second D/A converter (123) and a second other-side correction output to be applied to the first D/A converter (113); in that the first own-side correction output and the second other-side correction output are added by a first adder (112) and then applied to the first D/A converter; and in that the second own-side correction output and the first other-side correction

output are added by a second adder (122) and then applied to the second D/A converter.

4. A system as claimed in Claim 2 or Claim 3, characterised in that the receiver unit (200) includes a first demodulator and a second demodulator; in that the first demodulator comprises a first receiving-end A/D converter (213) to receive an analog level signal from the transmitter unit (100), a first receiving-end memory circuit (211) to receive the output from the first receiving-end A/D converter, and a first receiving-end adder (212) located between the first receiving-end A/D converter and the first receiving-end memory circuit, the first demodulator producing first digital output data (D'1) to be reproduced by an operation reverse to that carried out in said first level converter (111,113); and in that the second demodulator comprises a second receiving-end A/D converter (223) to receive the analog level signal from the transmitter unit, a second receiving-end memory circuit (221) to receive the output from the second receiving-end A/D converter, and a second receiving-end adder (222) located between the second receiving-end A/D converter and the second receiving-end memory circuit, the second demodulator producing second digital output data (D'2) to be reproduced by an operation reverse to that carried out in said second level converter (121,123).

5. A system as claimed in Claim 4, characterised in that the receiver unit (200) includes a data-error supervising circuit (55) for the first and second digital output data (D'1,D'2); in that the transmitter unit (100) includes a central processing unit (53) which receives, via a sub-transmission line (56), resultant information from the data-error supervising circuit and renews, according to the resultant information, the first and second digital correction outputs (d12,d22) by rewriting the contents of the first and second memory circuits (111,121) in the transmitter unit.

6. A system as claimed in Claim 5, characterised in that the data-error supervising circuit (55) comprises a parity checker.

7. A system as claimed in Claim 5, characterised in that the data-error supervising circuit (55) comprises a first integrator (64-1) to receive lower bits of the first digital output data (D'1), a first comparator (65-1) which compares the output level of the first integrator with a predetermined threshold level (Vth), a second integrator (64-2) to receive lower bits of the second digital output data (D'2), a second comparator (65-2) which compares the output level of the second integrator with the predetermined threshold level, an OR gate (66) to receive the outputs from the first and second comparators, a memory circuit (63) which is activated by the output from the OR gate and stores the upper bits of the first and second digital output data for feeding to the central processing unit (53).

8. A system as claimed in Claim 5, characterised in that the transmitter unit (100) includes first and second switch circuits (51,52), both controlled by the central processing unit (CPU),to provide selectively first and second test data (TD1,TD2) instead of the first and second digital input data (D1,D2), respectively.

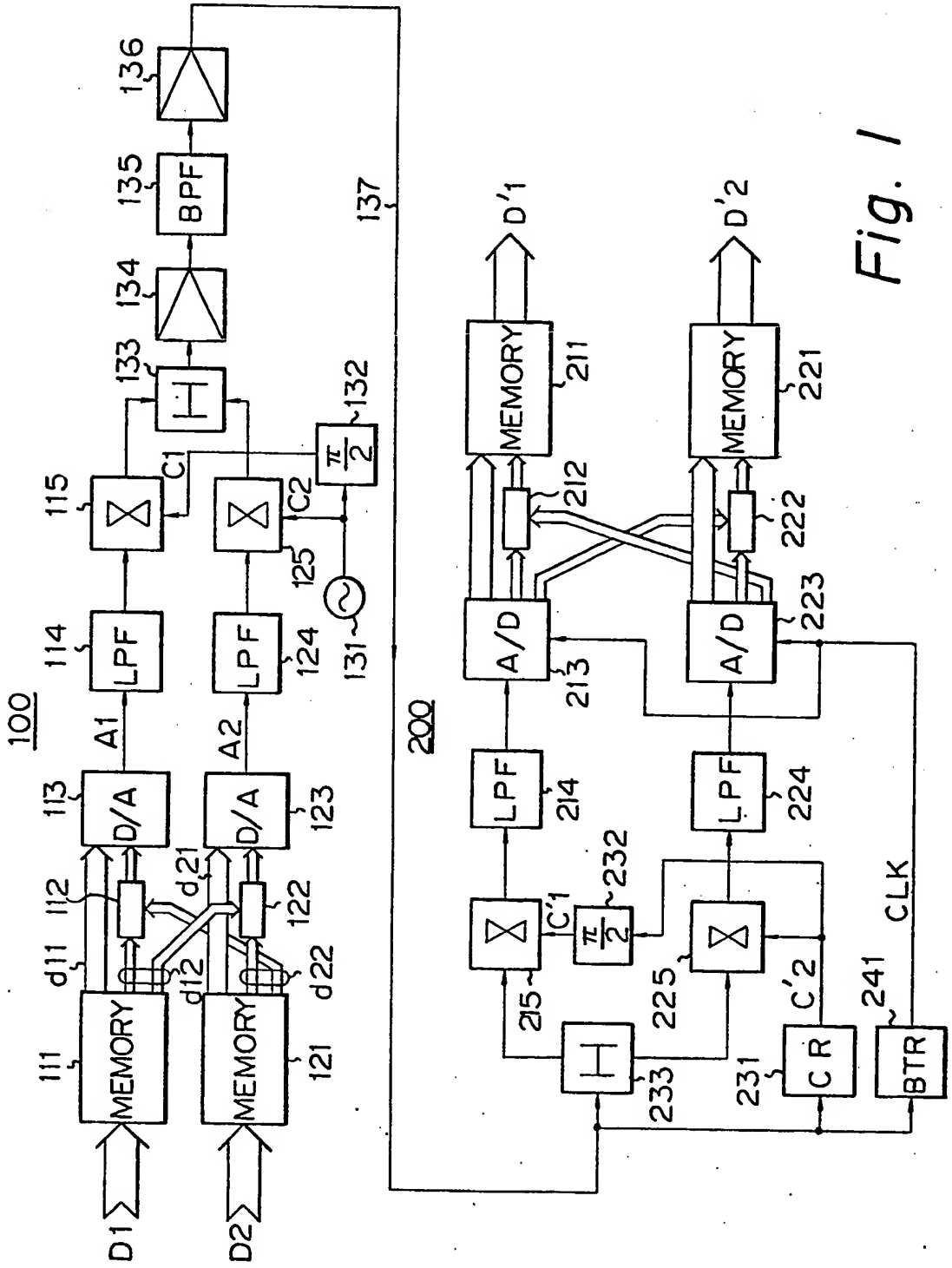


Fig. 1

Fig. 2

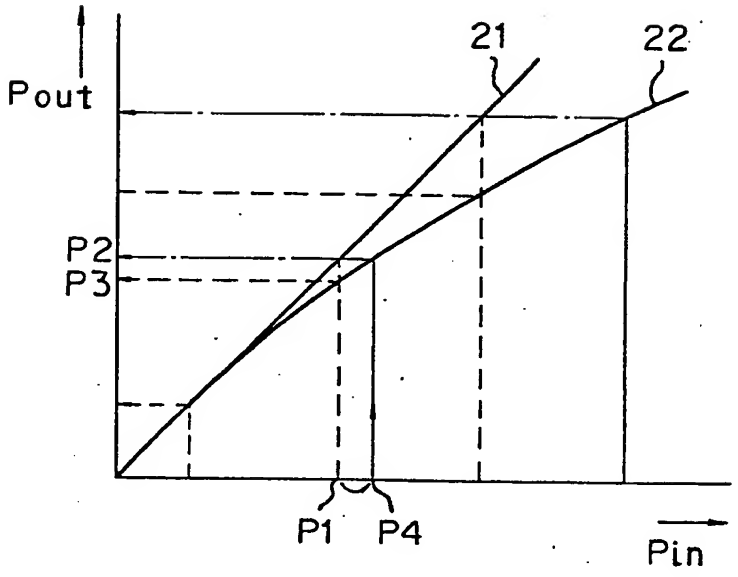


Fig. 3

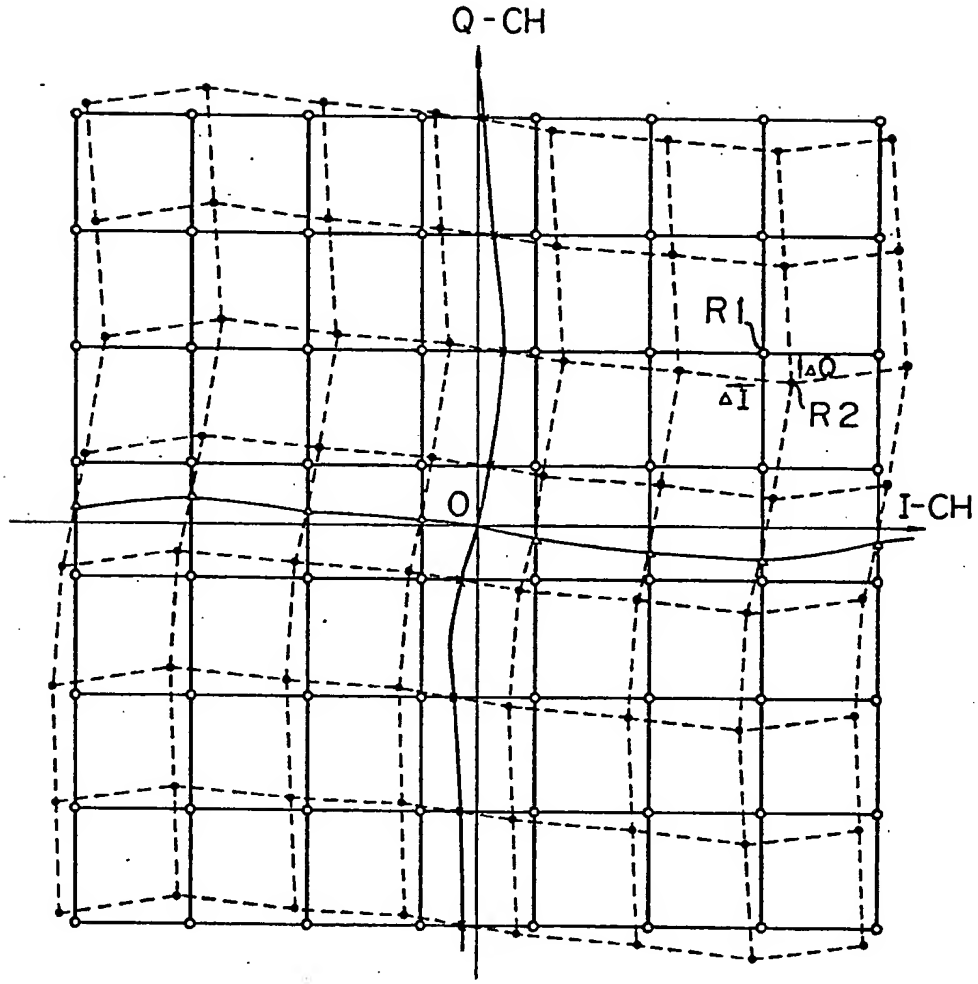


Fig. 4

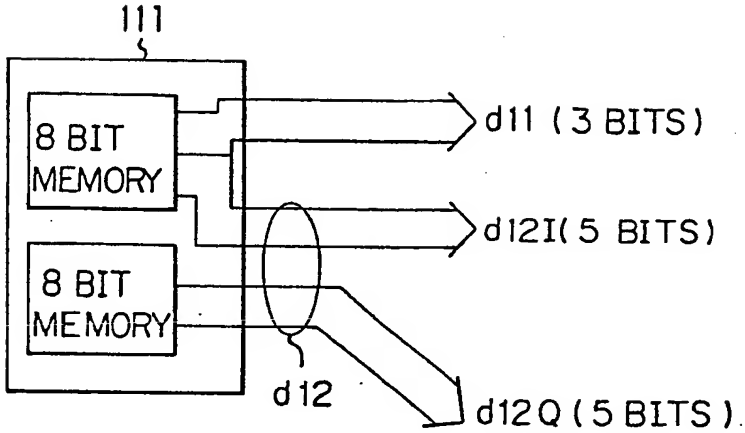

111
8 BIT MEMORY
8 BIT MEMORY
d11 (3 BITS)
d12I(5 BITS)
d12
d12Q (5 BITS)

Fig. 5

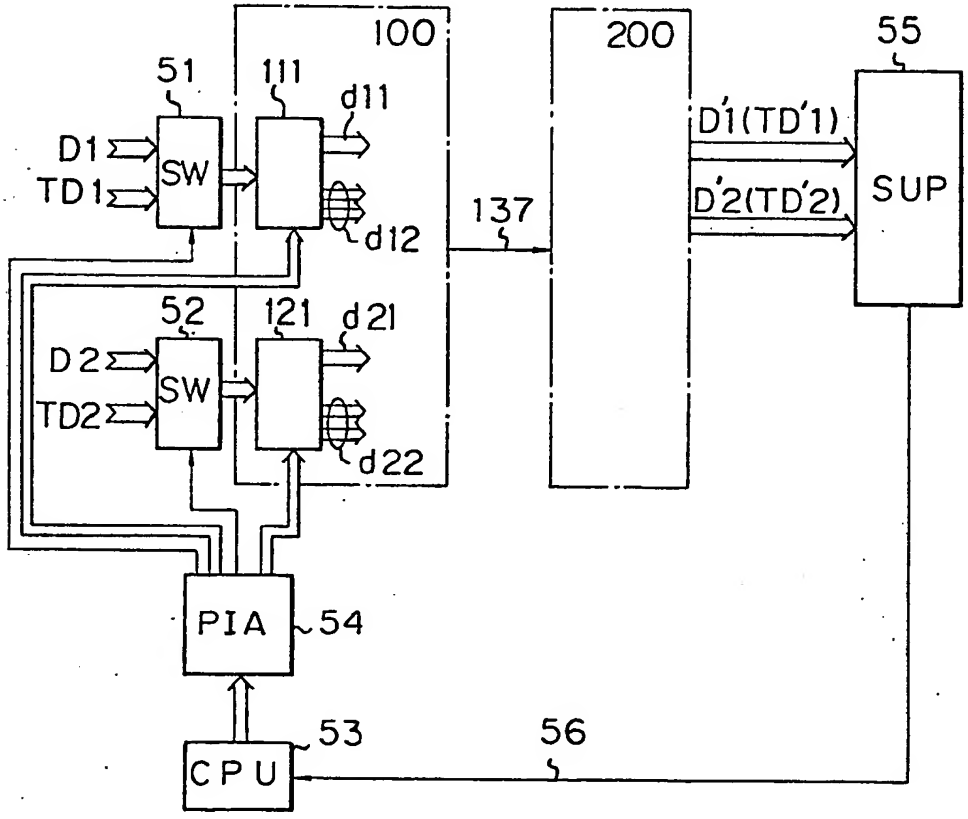
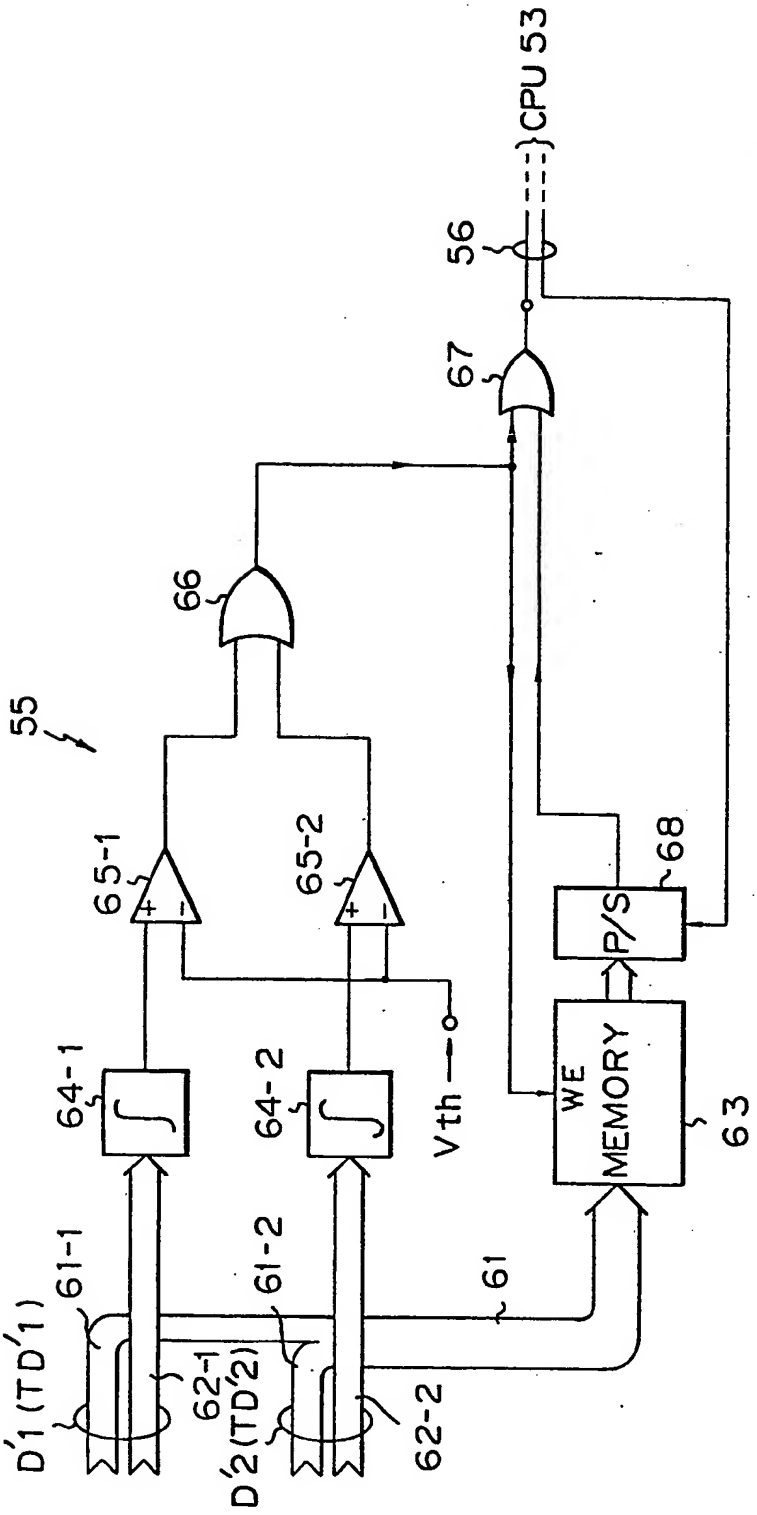

100
200
55
51
111
d11
D1
TD1
SW
d12
137
D'1(TD'1)
D'2(TD'2)
SUP
52
121
d21
D2
TD2
SW
d22
PIA
54
53
56
CPU

Fig. 6


CPU 53
56
67
66
55
65-1
65-2
68
P/S
WE
MEMORY
63
64-1
64-2
Vth
61-1
61-2
61
D'1 (TD'1)
62-1
D'2 (TD'2)
62-2